AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at line 2 of page 1 as follows:

This application is a continuation of U.S. Patent Application No. 10/279,004, issued as US Patent which was a continuation-in-part application of provisional application Ser. No. 60/330,596 filed October 25, 2001. It is also a continuation-in-part to the previous patents 5,696,458, 6,150,849 and 6,333,648 by the inventor. The entire disclosure of those related applications are incorporated herein by reference for all purposes.

Please amend the paragraph beginning at line 16 of page 33 as follows:

The major part of the power is consumed in the input transistor, where a large current is essential for the low noise. Throughout the rest of the analog and digital circuits, where lowering the power consumption will not effect the noise performance of the chip, circuits were developed with lowest possible power consumption for the selected fabrication process. Notably, one of the amplifier designs was found to generate excess noise and was replaced by a circuit that was both low power and low noise.

Channel power down available on a per channel basis. As stated in Table II, for a 1 kHz, single-hit event rate, the current estimate for the power consumption is 6 mW/ch with fast trigger path disabled. Disabled channels dissipate <0.5mW each. ~~Table VII (next page) shows the power dissipation distribution and the improvement achieved between the initial and current design.~~ We could clearly reduce power in the Diff buffer, the Shaper and the Fast shaper. However, with the fast path disabled, we will dissipate about 4.7mW per channel. This does not include power dissipation in other external circuits.